Claim Amendments

1.(Currently Amended) An apparatus comprising:

a modular multiplier including a plurality of independent computation channels, said plurality of independent computation channels including a first computation channel and a second computation channel each capable of performing an independent modular multiplication operation; and

a coupling device interposed between said first computation channel and said second computation channel to receive a first control signal and to couple said first computation channel to said second computation channel in response to a receipt of said first control signal.

2. (Original) The apparatus as set forth in claim 1, wherein said modular multiplier comprises a linear systolic array of processing elements, said linear systolic array of processing elements including said plurality of independent computation channels.

3. (Original) The apparatus as set forth in claim 1, wherein said coupling device comprises a coupling device to receive a second control signal and to selectively couple said first computation channel to said second computation channel in response to a state of said second control signal.

4. (Original) The apparatus as set forth in claim 3, said apparatus having a first mode of operation corresponding to a first state of said second control signal wherein

said first computation channel is operably separated from said second computation channel and a second mode of operation corresponding to a second state of said second control signal wherein said first computation channel is operably coupled to said second computation channel via said coupling device.

5. (Original) The apparatus as set forth in claim 4, wherein said first computation channel and said second computation channel operate as two n-bit modular multipliers in said first mode of operation and as a single 2n-bit modular multiplier in said second mode of operation, where n is an integer.

6. (Original) The apparatus as set forth in claim 5, where n is 512.

7. (Original) The apparatus as set forth in claim 1, wherein said modular multiplier comprises a Montgomery multiplier.

8. (Original) The apparatus as set forth in claim 1, wherein said a coupling device comprises a first multiplexer coupled between an output of said first computation channel and an input of said second computation channel and a second multiplexer coupled between an output of said second computation channel and an input of said first computation channel.

9. (Currently Amended) A processor comprising:

a modular multiplier including a plurality of independent computation channels, said plurality of independent computation channels including a first computation channel

and a second computation channel each capable of performing an independent modular multiplication operation; and

a coupling device interposed between said first computation channel and said second computation channel to receive a first control signal and to couple said first computation channel to said second computation channel in response to a receipt of said first control signal.

10. (Original) The processor as set forth in claim 9, wherein said modular multiplier comprises a linear systolic array of processing elements, said linear systolic array of processing elements including said plurality of independent computation channels.

11. (Original) The processor as set forth in claim 9, wherein said coupling device comprises a coupling device to receive a second control signal and to selectively couple said first computation channel to said second computation channel in response to a state of said second control signal.

12. (Original) The processor as set forth in claim 11, said processor having a first mode of operation corresponding to a first state of said second control signal wherein said first computation channel is operably separated from said second computation channel and a second mode of operation corresponding to a second state of said second control signal wherein said first computation channel is operably coupled to said second computation channel via said coupling device.

13. (Original) The processor as set forth in claim 12, wherein said first computation channel and said second computation channel operate as two n-bit modular multipliers in said first mode of operation and as a single 2n-bit modular multiplier in said second mode of operation, where n is an integer.

14. (Original) The processor as set forth in claim 13, where n is 512.

15. (Original) The processor as set forth in claim 9, wherein said modular multiplier comprises a Montgomery multiplier.

16. (Original) The processor as set forth in claim 9, wherein said a coupling device comprises a first multiplexer coupled between an output of said first computation channel and an input of said second computation channel and a second multiplexer coupled between an output of said second computation channel and an input of said first computation channel.

17. (Currently Amended) A system comprising:

a memory to store data and instructions;

a first processor coupled to said memory to process data and execute instructions;

a second processor coupled to said memory, said second processor comprising:

a modular multiplier including a plurality of independent computation channels, said plurality of independent computation channels including a first computation channel

and a second computation channel each capable of performing an independent modular multiplication operation; and

a coupling device interposed between said first computation channel and said second computation channel to receive a first control signal and to couple said first computation channel to said second computation channel in response to a receipt of said first control signal.

18. (Original) The system as set forth in claim 17, wherein said modular multiplier comprises a linear systolic array of processing elements, said linear systolic array of processing elements including said plurality of independent computation channels.

19. (Original) The system as set forth in claim 17, wherein said coupling device comprises a coupling device to receive a second control signal and to selectively couple said first computation channel to said second computation channel in response to a state of said second control signal.

20. (Original) The system as set forth in claim 19, said second processor having a first mode of operation corresponding to a first state of said second control signal wherein said first computation channel is operably separated from said second computation channel and a second mode of operation corresponding to a second state of said second control signal wherein said first computation channel is operably coupled to said second computation channel via said coupling device.

21. (Original) The system as set forth in claim 20, wherein said first computation channel and said second computation channel operate as two n-bit modular multipliers in said first mode of operation and as a single 2n-bit modular multiplier in said second mode of operation, where n is an integer.

22. (Original) The system as set forth in claim 17, wherein said a coupling device comprises a first multiplexer coupled between an output of said first computation channel and an input of said second computation channel and a second multiplexer coupled between an output of said second computation channel and an input of said first computation channel.

23. (Currently Amended) A method comprising:

receiving a first control signal and a plurality of operands; and

performing a modular multiplication operation on said plurality of operands utilizing a modular multiplier including a plurality of independent computation channels, said plurality of independent computation channels including a first computation channel and a second computation channel <u>each capable of performing an independent modular multiplication operation</u>, wherein performing said modular multiplication operation comprises:

coupling said first computation channel with said second computation channel in response to receiving said first control signal;

performing a first portion of said modular multiplication operation utilizing said first computation channel; and

performing a second portion of said modular multiplication operation utilizing said second computation channel.

24. (Original) The method as set forth in claim 23, wherein performing a modular multiplication operation comprises performing a modular multiplication operation on said plurality of operands utilizing a modular multiplier including a linear systolic array of processing elements, said linear systolic array of processing elements including said plurality of independent computation channels.

25. (Original) The method as set forth in claim 23, wherein:

performing a first portion of said modular multiplication operation comprises providing said plurality of operands to said first computation channel and processing said plurality of operands utilizing said first computation channel to produce an intermediate result;

coupling said first computation channel with said second computation channel comprises providing said intermediate result to said second computation channel; and

performing a second portion of said modular multiplication operation comprises processing said intermediate result utilizing said second computation channel.

26. (Original) The method as set forth in claim 23, said method further comprising receiving a second control signal, wherein coupling said first computation channel with said second computation channel comprises selectively coupling said first computation channel with said second computation channel in response to receiving said second control signal.

27. (Currently Amended) A machine-readable medium having a plurality of machine-executable instructions embodied therein which when executed by a machine, cause said machine to perform a method comprising:

receiving a first control signal and a plurality of operands; and

performing a modular multiplication operation on said plurality of operands utilizing a modular multiplier including a plurality of independent computation channels, said plurality of independent computation channels including a first computation channel and a second computation channel each capable of performing an independent modular multiplication operation, wherein performing said modular multiplication operation comprises:

coupling said first computation channel with said second computation channel in response to receiving said first control signal;

performing a first portion of said modular multiplication operation utilizing said first computation channel; and

performing a second portion of said modular multiplication operation utilizing said second computation channel.

28. (Original) The machine-readable medium as set forth in claim 27, wherein performing a modular multiplication operation comprises performing a modular multiplication operation on said plurality of operands utilizing a modular multiplier including a linear systolic array of processing elements, said linear systolic array of processing elements including said plurality of independent computation channels.

29. (Original) The machine-readable medium as set forth in claim 27, wherein:

performing a first portion of said modular multiplication operation comprises providing said plurality of operands to said first computation channel and processing said plurality of operands utilizing said first computation channel to produce an intermediate result;

coupling said first computation channel with said second computation channel comprises providing said intermediate result to said second computation channel; and

performing a second portion of said modular multiplication operation comprises processing said intermediate result utilizing said second computation channel.

30. (Original) The machine-readable medium as set forth in claim 27, said method further comprising receiving a second control signal, wherein coupling said first computation channel with said second computation channel comprises selectively coupling said first computation channel with said second computation channel in response to receiving said second control signal.

31. (Canceled).

32. (Currently Amended) ~~The method of claim 31~~ A method comprising:

receiving a data value at a first end of a systolic array multiplier from a second end of the systolic array multiplier, wherein receiving a data value at a first end of a systolic array multiplier from a second end of the systolic array multiplier comprises:

receiving a data value from a second end of the systolic array multiplier at a first input of a multiplexer;

receiving a channel data input signal at a second input of the multiplexer; and

providing either the data value from the second end of the systolic array multiplier or the channel data input signal to the first end of a systolic array multiplier via an output of the multiplexer.

33. (Currently Amended) The method of claim ~~31~~ 32, further comprising:

processing data in processing elements, which operate on a given problem during alternating cycles of a clock signal.

34. (New) The apparatus as set forth in claim 1, wherein said first computation channel and said second computation channel operate as two modular multipliers in a first mode of operation and as a single modular multiplier in a second mode of operation.

35. (New) The processor as set forth in claim 9, wherein said first computation channel and said second computation channel operate as two modular multipliers in a first mode of operation and as a single modular multiplier in a second mode of operation.

36. (New) The system as set forth in claim 17, wherein said first computation channel and said second computation channel operate as two modular multipliers in a first mode of operation and as a single modular multiplier in a second mode of operation.